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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/560,364	04/28/2000	Karen Lo	10002496-1	3565

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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2634	

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12

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/560,364	LO ET AL.	
	Examiner	Art Unit	
	Jason M Perilla	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 16-44 are pending in the instant application following the entry of the amendment filed May 12, 2004.

Claim Objections

2. Claims 16 and 35 are objected to because of the following informalities:

Regarding claims 16 and 35, the limitation, "configured to halt each said data strobe" should be replaced by –configured to halt said at least one data strobe—to maintain consistency in the claim language.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 16-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nikel ("Low Cost 400Mhz Source Synchronous Data Links") in view of Keeth et al (US 6026051 – previously cited; hereafter "Keeth").

Regarding claim 16, Nikel discloses a source synchronous link (title) comprising: a communication link; a source synchronous transmitter (source synchronous driver SSD) constructed and arranged to transmit a data signal and at least one data strobe signal over said communication link (differential signals); and a source synchronous receiver (source synchronous receiver SSR), coupled to said communication link, that

clocks in said data signal (latching data) in accordance with said at least one data strobe signal (pg. 147, lines 3-17). Nikel fully discloses the components of a source synchronous communications link comprising the transmitter which transmits data and a differential strobe as well as the receiver which receives the data and latches it according to the received strobe signal. It is inherent that there is a communications link between the receiver and the transmitter. Nikel does not disclose that (a) the transmitter is configured to halt the at least one data strobe signal in a selected logical state in response to an external condition or (b) when the at least one data strobe signal is halted, the data signal is not clocked into the source synchronous receiver. One skilled in the art is aware that the limitations of (b) are inherent in the source synchronous link of Nikel. Nikel discloses that the data is latched into the receiver according to the data strobe signal. Therefore, it is inherent that if the data strobe signal has been halted, the "data latching" of data at the side of the receiver will be halted as well. Further, Keeth teaches the limitations of (b) by figure 3. Keeth discloses a differential data strobe transmitter (fig. 3) for transmitting over a source synchronous communication link a differential strobe comprising a data strobe signal (DCLK0OUT), an inverse data strobe signal (DCLK0OUT*) and strobe stopping logic (fig. 3, ref. 36, 44) configured to control signal level states used by said signal generator logic (fig. 3, ref. 38, 40, 46, & 48) to cause said data strobe signal and said inverse data strobe signal to remain halted in a selected logical state (col. 3, lines 45-51; col. 4, lines 49-65). While figure 3 of Keeth is embodied as a differential strobe receiver, it would be obvious to use such a configuration as a differential strobe transmitter. Further the "differential

strobe receiver" of Keeth can be considered a "differential strobe transmitter" because it provides the differential clock signals to the remaining areas of the receiver. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a differential strobe transmitter as taught by Keeth in the link of Nikel because the strobes could be halted in a selected state to prevent the latching of data at the side of the receiver.

Regarding claim 17, Nikel in view of Keeth disclose the limitations of claim 16 as applied above. Further, Nikel discloses that said source synchronous receiver comprises data capture flip-flops (data latches) controlled by said one or more data strobe signals, wherein when said at least one data strobe signal is halted, subsequently-received data signals are not written to said data capture flip-flops (pg. 147, lines 3-17). Nikel discloses that the data is latched into the receiver according to the data strobe signal. Therefore, it is inherent that if the data strobe signal has been halted, the "data latching" of data at the side of the receiver will be halted as well.

Regarding claim 18, Nikel in view of Keeth disclose the limitations of claim 16 as applied above. Further the link of Nikel in view of Keeth discloses that the source synchronous transmitter comprises: data strobe transmit logic (fig. 3 of Keeth, refs. 50 and 42) configured to transmit said at least one data strobe signal over at least one clock line of said communication link, and to maintain said at least one data strobe signal in a selected logical state (col. 3, lines 45-51; col. 4, lines 49-65) in response to said external condition (enable*).

Regarding claim 19, Nikel in view of Keeth disclose the limitations of claim 16 as applied above. Further, it is inherent that the link of Nikel in view of Keeth comprises data transmit logic configured to transmit said data signal over a data line of said communication link.

Regarding claim 20, Nikel in view of Keeth disclose the limitations of claim 18 as applied above. Further, Keeth discloses by figure 3 that the at least one data strobe signal comprises: a first data strobe signal (DCLK0OUT); and a second data strobe signal (DCLK0OUT*) transmitted with a phase opposite a phase of said first data strobe signal. The asterisk (*) of DCLK0OUT* represents an inverse or opposite phase relative to DCLK0OUT. Further, this is inherent in view of the term "differential" regarding strobes disclosed by Nikel.

Regarding claim 21, Nikel in view of Keeth disclose the limitations of claim 20 as applied above. Further, in the link of Nikel in view of Keeth the first data strobe signal and the second data strobe signal are each generated as single ended bits that are opposite in phase with each other as applied to claim 20 above.

Regarding claim 22, Nikel in view of Keeth disclose the limitations of claim 20 as applied above. Further, Keeth discloses that said data strobe transmit logic comprises: a differential data strobe signal generator (fig. 3) configured to select from a first two available signals (1 and 4 below) to generate said first data strobe signal (DCLK0OUT*) and to select from a second two available signals (2 and 3 below) to generate said second data strobe signal (DCLK0OUT). Figure 3 shows the differential strobe signal generator logic (ref. 38, 40, 46, & 48) having four applied signals (2 each per strobe

output) used to generate the two differential data strobe signals. The 4 applied signals shown in figure 3 are:

1.) The output of inverter 36.

2.) The output of inverter 44.

3.) VCC connected to MUX 46.

4.) GND connected to MUX 40.

Keeth discloses that the two differential strobe outputs are each generated by selecting alternately between two of the applied signal levels (col. 3, line 45 – col. 4, line 65). Keeth further discloses strobe stopping logic (enable*, 36, and 44) that controls logic levels of said first two available signals and said second two available signals, when; in to halt said at least one data strobe signal said strobe stopping logic sets said first two available signals to a same first logic level (GND – logic 0) and sets said second two available signals to a same second logic level (VCC – logic 1) different than said first same logic level. The enable* signal directly results in the setting of the first two signals to be of the same logic level 0, and also directly results in the setting of the second two signals to be of the same logic level 1.

Regarding claim 23, Nikel in view of Keeth disclose the limitations of claim 16 as applied above. Further, Keeth discloses by figure 3 that the at least one data strobe signal comprises: a first data strobe signal (DCLK0OUT); and a second data strobe signal (DCLK0OUT*) transmitted with a phase opposite a phase of said first data strobe signal. The asterisk (*) of DCLK0OUT* represents an inverse or opposite phase relative

to DCLK0OUT. Further, this is inherent in view of the term "differential" regarding strobes disclosed by Nikel.

Regarding claim 24, Nikel in view of Keeth disclose the limitations of claim 23 as applied above. Further, Keeth discloses that said first data strobe signal and said second data strobe signal may be transmitted at either one of two logical states and wherein said data strobe transmit logic maintains said first data strobe signal at a first of said two logical states and maintains said second data strobe signal at a second of said two logical states when said data strobe transmit logic halts said one or more data strobe signals as applied above in claims 16, 20, 21, and 23.

Regarding claim 25, Nikel in view of Keeth disclose the limitations of claim 16 as applied above. Further, Keeth discloses the link wherein when operating in a normal mode of operation (enable* = true) said source synchronous transmitter toggles said first data strobe signal between two logical states (VCC or logic 1 and logic 0), and toggles said second data strobe signal between the two logical states (logic 1 and GND or logic 0), and wherein when operating in a data capture debug mode of operation (enable* = false), said source synchronous transmitter halts said first data strobe signal at one of said two logical states (logic 1), and halts said second data strobe signal at the other one of said two logical states (logic 0). Keeth discloses that the two differential strobe outputs are each generated by selecting alternately between two of the applied signal levels (col. 3, line 45 – col. 4, line 65). Keeth further discloses strobe stopping logic (enable*, 36, and 44) that controls logic levels of said first two available signals and said second two available signals, when; in to halt said at least one data strobe

signal said strobe stopping logic sets said first two available signals to a same first logic level (GND – logic 0) and sets said second two available signals to a same second logic level (VCC – logic 1) different than said first same logic level.

Regarding claim 26, Nikel in view of Keeth disclose, as applied to claim 16 above, a circuit comprising: a communication link; a first processing core comprising a source synchronous transmitter constructed and arranged to transmit a data signal and at least one data strobe signal over said communication link, wherein said transmitter is configured to halt said at least one data strobe signal in a selected logical state in response to an external condition; and a second processing core comprising a source synchronous receiver, coupled to said communication link, that clocks in said data signal in accordance with said at least one data strobe signal, wherein when said at least one data strobe signal is halted, said data signal is not clocked into said source synchronous receiver. *Further, the first processing core or application specific integrated circuit (ASIC) and the second processing core or ASIC are disclosed by Nikel as being connected by the source synchronous data link (pg. 146, lines 8-10).*

Regarding claims 27-34, Nikel in view of Keeth disclose the limitations of the claims as applied to claims 17-24, respectively, above.

Regarding claims 35-40, Nikel in view of Keeth disclose the limitations of the claims as applied to claims 16-18, and 20-22, respectively, above.

Regarding claims 41-44, Nikel in view of Keeth disclose the limitations of the claims as applied to claims 16, 17, 20 and 22, respectively, above.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M Perilla whose telephone number is (703) 305-0374. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Chin can be reached on (703) 305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
August 10, 2004

jmp

CHIEH M. FAN
PRIMARY EXAMINER